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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,756	01/14/2004	Hajime Kimura	12732-207001 / US6910	1526

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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,756	KIMURA ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-80* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/04, 7/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the abstract should avoid phrases such as, "the invention is characterized in that..." (see Page 45, Line 6 of the instant application). Correction is required. See MPEP § 608.01(b).

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "130" has been used to designate both a switch and a current line (see Page 5, Lines 11-17 of the instant application). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any

amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 3 is objected to because of the following informalities: "shift resistor" should be changed to "shift register" (see line 3, for instance). Appropriate correction is required.

6. Applicant is advised that should claim 78 be found allowable, claim 79 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 19 recites the limitation "each certain period" in the last line. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1, 2, 19, and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishizuka et al (US 5,923,309 A).

Regarding claim 1, Ishizuka discloses a current source circuit [Fig. 8; 3a] characterized in by comprising a plurality of current sources [Fig. 8; 3_{a1}-3_{a2}] which can control an output current value [Fig. 8; I, 2I, 4I] by a set signal inputted from outside [Fig. 7; 1], wherein a changing over means [Fig. 8; SW_0-SW_3] which can change over an electrical connection between an output line [Fig. 8; X_1-X_2] and the plurality of current sources is provided between the output line and the plurality of current sources (see Column 5, Lines 7-43).

Regarding claim 2, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Ishizuka discloses a plurality of pairs [Fig. 8; SW_0-SW_3] of current sources [Fig. 8; 3_{a1}-3_{a2}] (see Column 5, Lines 7-43).

Regarding claim 19, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Ishizuka discloses a driving method of a signal line driver circuit characterized in by comprising a current source circuit [Fig. 8; 3a] comprising a plurality of current sources [Fig. 8; 3_{a1}-3_{a2}], a means [Fig. 7; 1] for setting a current [Fig. 8; I, 2I, 4I] of the plurality of current sources, a plurality of signal lines [Fig. 8; X_1-X_2] through which the set current flows, and a changing over means [Fig. 8; SW_0-SW_3] provided between the signal line and the current source, wherein the changing over means changes over a connection of the signal line and the current source circuit in each certain period (see Column 5, Lines 7-43).

Regarding claim 24, Ishizuka discloses a period for performing a set operation by a means [Fig. 7; 1] for setting a current of the plurality of current sources is provided in the certain period (see Column 5, Lines 7-43).

Regarding claim 25, Ishizuka discloses an operation to change over an electrical connection between the signal line and the current source and the set operation are not overlapped with each other in the certain period (see Column 5, Lines 7-43).

Regarding claim 26, Ishizuka discloses the operation to change over an electrical connection between the signal line and the current source is provided after the set operation in the certain period (see Column 5, Lines 7-43).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3-18, 20-23, and 27-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizuka et al (US 5,923,309 A) in view of Yamada et al (US 5,990,629 A).

Regarding claim 3, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Ishizuka discloses a signal line driver circuit [Fig. 8; 3a] (see Column 5, Lines 7-43). Ishizuka does not explicitly teach a shift register or latch circuitry.

However, Yamada does disclose a signal line driver circuit [Fig. 1; 4] characterized in by comprising a shift register [Fig. 7; 41], a first latch circuit [Fig. 7; 42], and a second latch circuit [Fig. 7; 43] (see Column 12, Line 28 - Column 13, Line 12). Ishizuka and Yamada are analogous art, because they are both from the shared field of electroluminescent display devices and driving methods. Therefore, it would have been obvious to one skilled in the art at the time of invention to use Yamada's control circuitry with Ishizuka's pixel drive circuitry, so as to obtain excellent light emission luminance gradation even for light-emitting elements having different patterns.

Regarding claim 4, this claim is rejected by the reasoning applied in rejecting claims 1 and 3; furthermore, Ishizuka discloses switches [Fig. 8; SW_0-SW_3 & SW_{a1}-SW_{a2}] provided in the plurality of current sources (see Column 5, Lines 7-43).

Regarding claim 5, this claim is rejected by the reasoning applied in rejecting claims 1 and 3.

Regarding claim 6, this claïm is rejected by the reasoning applied in rejecting claims 1, 3, 4, and 5.

Regarding claim 7, this claim is rejected by the reasoning applied in rejecting claims 1 and 3; furthermore, Yamada discloses a first and second shift registers [Fig. 7; 41] (see Column 12, Line 28 - Column 13, Line 12 -- wherein shift register circuitry 41 is constituted by plural shift register stages, one for each separate output line).

Regarding claim 8, this claim is rejected by the reasoning applied in rejecting claims 1, 3, 4, and 7.

Regarding claim 9, this claim is rejected by the reasoning applied in rejecting claims 1 and 3; furthermore, Ishizuka discloses a plurality of first and second current sources [Fig. 8; 3_{a1}-3_{a2}] which can control an output current value [Fig. 8; I, 2I, 4I] by a set signal inputted from

outside [Fig. 7; 1], wherein a changing over means [Fig. 8; SW_0-SW_3] which can change over an electrical connection between a signal line [Fig. 8; X_1-X_2] and the plurality of first and second current sources is provided between the signal line and the plurality of first and second current sources (see Column 5, Lines 7-43).

Regarding claim 10, this claim is rejected by the reasoning applied in rejecting claims 1, 3, 4, and 9; furthermore, Ishizuka discloses first and second switches [Fig. 8; SW_0-SW_3 & SW_{a1}-SW_{a2}] (see Column 5, Lines 7-43).

Regarding claim 11, this claim is rejected by the reasoning applied in rejecting claims 1, 2, 3, and 9.

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claims 1, 2, 3, 4, 9, and 10.

Regarding claim 13, Ishizuka discloses the changing over means comprises a plurality of analog switches [Fig. 8; SW_0-SW_3 & SW_{a1}-SW_{a2}], and that the current source is connected to the signal line through the analog switch (see Column 5, Lines 7-43).

Regarding claim 14, Ishizuka discloses the changing over means comprises three analog switches [Fig. 8; SW_0-SW_3 & SW_{a1}-SW_{a2}] for each of the signal line [Fig. 8; X_1-X_2], and that the

each of the three analog switches is connected to the different current sources [Fig. 8; 3_{a1}-3_{a2}] (see Column 5, Lines 7-43).

Regarding claim 15, Ishizuka discloses the changing over means comprises a group of analog switches [Fig. 8; SW_0-SW_3 & SW_{a1}-SW_{a2}] formed by a plurality of analog switches and a group of current source circuits [Fig. 8; 3_{a1}-3_{a2}] formed by a plurality of the current sources (see Column 5, Lines 7-43).

Regarding claim 16, Ishizuka discloses a light emitting device [Fig. 8; 4] characterized in by comprising the signal line driver circuit (see Column 5, Lines 7-43).

Regarding claim 17, Ishizuka discloses a light emitting device [Fig. 8; 4] characterized in by comprising two of the signal line driver circuits [Fig. 8; 3_{a1}-3_{a2}] and a pixel portion [Fig. 8; E1-E4], wherein the two signal line driver circuits have a function to input a difference of currents supplied from current sources of each to the pixel portion (see Column 5, Lines 7-43).

Regarding claim 18, Ishizuka discloses a light emitting device [Fig. 8; 4] characterized in by comprising the signal line driver circuit [Fig. 8; 3_{a1}-3_{a2}] and a pixel portion [Fig. 8; E1-E4], wherein in the pixel portion, the signal line and a plurality of scan lines are aligned in matrix [Fig. 8; 4, wherein a light emitting element is disposed at an intersection of the signal line [Fig. 8; X_1-X_2] and the scan line [Fig. 8; Y_1-Y_2], and wherein a transistor [Fig. 8; SW_{Y1}-SW_{3Y2}] for switching which controls a current from the signal line and a transistor [Fig. 8; SW_0-SW_3 &

SW_{a1}-SW_{a2}] for controlling current which controls a current to be supplied to the light emitting element are provided (see Column 5, Lines 7-43).

Regarding claim 20, Yamada discloses the certain period is provided in a unit of frame period corresponding to a synchronized timing of a video signal inputted to the signal line (see Fig. 25; Column 37, Line 5 - Column 38, Line 8).

Regarding claim 21, Yamada discloses a unit of frame period corresponding to a synchronized timing of a video signal inputted to the signal line comprises a write period, and wherein the certain period is provided so as not to overlap the write period (see Fig. 25; Column 37, Line 5 - Column 38, Line 8).

Regarding claim 22, Yamada discloses a unit of frame period corresponding to a synchronized timing of a video signal inputted to the signal line comprises m (m is a natural number of 2 or more -- three subframes, for instance) subframe periods SF1, SF2, . . . , SFm, and that the certain period is provided in the subframe period (see Fig. 25; Column 37, Line 5 - Column 38, Line 8).

Regarding claim 23, Yamada discloses a unit of frame period corresponding to a synchronized timing of a video signal inputted to the signal line comprises m (m is a natural number of 2 or more -- three subframes, for instance) subframe periods SF1, SF2, . . . , SFm, and the subframe periods SF1, SF2, . . . , SFm each comprises write periods Ta1, Ta2, . . . , Tam

and display periods Ts1, Ts2, . . . , Tsm, and that the certain period is provided in the subframe period (see Fig. 25; Column 37, Line 5 - Column 38, Line 8).

Regarding claim 27, this claim is rejected by the reasoning applied in rejecting claim 13.

Regarding claim 28, this claim is rejected by the reasoning applied in rejecting claim 13.

Regarding claim 29, this claim is rejected by the reasoning applied in rejecting claim 13.

Regarding claim 30, this claim is rejected by the reasoning applied in rejecting claim 13.

Regarding claim 31, this claim is rejected by the reasoning applied in rejecting claim 13.

Regarding claim 32, this claim is rejected by the reasoning applied in rejecting claim 13.

Regarding claim 33, this claim is rejected by the reasoning applied in rejecting claim 13.

Regarding claim 34, this claim is rejected by the reasoning applied in rejecting claim 13.

Regarding claim 35, this claim is rejected by the reasoning applied in rejecting claim 13.

Regarding claim 36, this claim is rejected by the reasoning applied in rejecting claim 14.

Regarding claim 37, this claim is rejected by the reasoning applied in rejecting claim 14.

Regarding claim 38, this claim is rejected by the reasoning applied in rejecting claim 14.

Regarding claim 39, this claim is rejected by the reasoning applied in rejecting claim 14.

Regarding claim 40, this claim is rejected by the reasoning applied in rejecting claim 14.

Regarding claim 41, this claim is rejected by the reasoning applied in rejecting claim 14.

Regarding claim 42, this claim is rejected by the reasoning applied in rejecting claim 14.

Regarding claim 43, this claim is rejected by the reasoning applied in rejecting claim 14.

Regarding claim 44, this claim is rejected by the reasoning applied in rejecting claim 14.

Regarding claim 45, this claim is rejected by the reasoning applied in rejecting claim 15.

Regarding claim 46, this claim is rejected by the reasoning applied in rejecting claim 15.

Regarding claim 47, this claim is rejected by the reasoning applied in rejecting claim 15.

Regarding claim 48, this claim is rejected by the reasoning applied in rejecting claim 15.

Regarding claim 49, this claim is rejected by the reasoning applied in rejecting claim 15.

Regarding claim 50, this claim is rejected by the reasoning applied in rejecting claim 15.

Regarding claim 51, this claim is rejected by the reasoning applied in rejecting claim 15.

Regarding claim 52, this claim is rejected by the reasoning applied in rejecting claim 15.

Regarding claim 53, this claim is rejected by the reasoning applied in rejecting claim 15.

Regarding claim 54, this claim is rejected by the reasoning applied in rejecting claim 16.

Regarding claim 55, this claim is rejected by the reasoning applied in rejecting claim 16.

Regarding claim 56, this claim is rejected by the reasoning applied in rejecting claim 16.

Regarding claim 57, this claim is rejected by the reasoning applied in rejecting claim 16.

Regarding claim 58, this claim is rejected by the reasoning applied in rejecting claim 16.

Regarding claim 59, this claim is rejected by the reasoning applied in rejecting claim 16.

Regarding claim 60, this claim is rejected by the reasoning applied in rejecting claim 16.

Regarding claim 61, this claim is rejected by the reasoning applied in rejecting claim 16.

Regarding claim 62, this claim is rejected by the reasoning applied in rejecting claim 16.

Regarding claim 63, this claim is rejected by the reasoning applied in rejecting claim 17.

Regarding claim 64, this claim is rejected by the reasoning applied in rejecting claim 17.

Regarding claim 65, this claim is rejected by the reasoning applied in rejecting claim 17.

Regarding claim 66, this claim is rejected by the reasoning applied in rejecting claim 17.

Regarding claim 67, this claim is rejected by the reasoning applied in rejecting claim 17.

Regarding claim 68, this claim is rejected by the reasoning applied in rejecting claim 17.

Regarding claim 69, this claim is rejected by the reasoning applied in rejecting claim 17.

Regarding claim 70, this claim is rejected by the reasoning applied in rejecting claim 17.

Regarding claim 71, this claim is rejected by the reasoning applied in rejecting claim 17.

Regarding claim 72, this claim is rejected by the reasoning applied in rejecting claim 18.

Regarding claim 73, this claim is rejected by the reasoning applied in rejecting claim 18.

Regarding claim 74, this claim is rejected by the reasoning applied in rejecting claim 18.

Regarding claim 75, this claim is rejected by the reasoning applied in rejecting claim 18.

Regarding claim 76, this claim is rejected by the reasoning applied in rejecting claim 18.

Regarding claim 77, this claim is rejected by the reasoning applied in rejecting claim 18.

Regarding claim 78, this claim is rejected by the reasoning applied in rejecting claim 18.

Regarding claim 79, this claim is rejected by the reasoning applied in rejecting claim 18.

Regarding claim 80, this claim is rejected by the reasoning applied in rejecting claim 18.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. McDonald (US 3,696,393 A), Norman et al (US 5,719,589 A), Nairn (US 6,037,888 A), Kawashima et al (US 6,091,203 A), Song et al (US 6,331,830 B1), Chung et al (US 6,339,391 B1), Yoshida et al (US 6,351,076 B1), Suzuki (US 6,369,786 B1), Tsuchida et al (US 6,473,064 B1), Inagaki et al (US 6,590,516 B2), Kudo et al (US 6,753,880 B2), and Koyama et al (JP 2002207465 A) are cited to further evidence the state of the art pertaining to current source circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J.P.
20 June 2005

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